

100

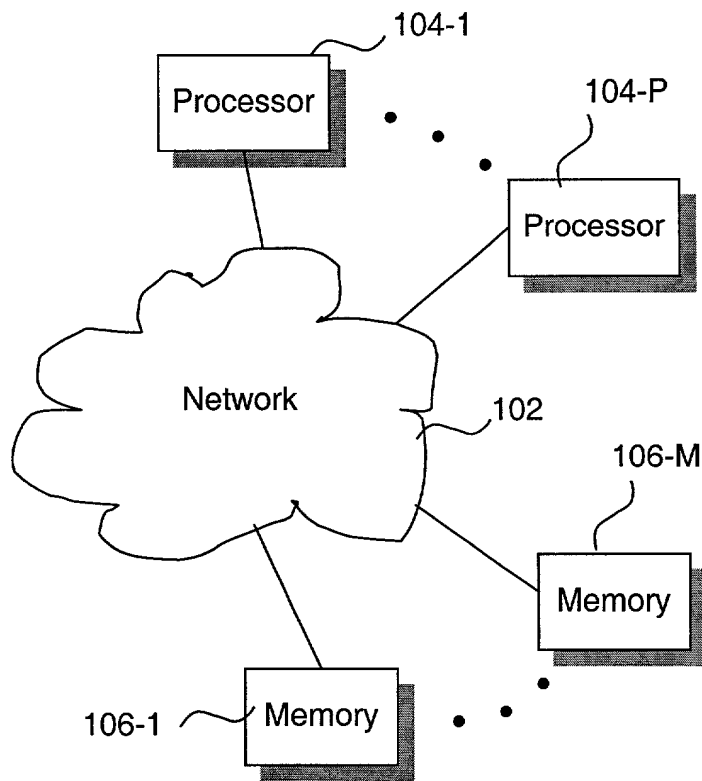


FIG. 1

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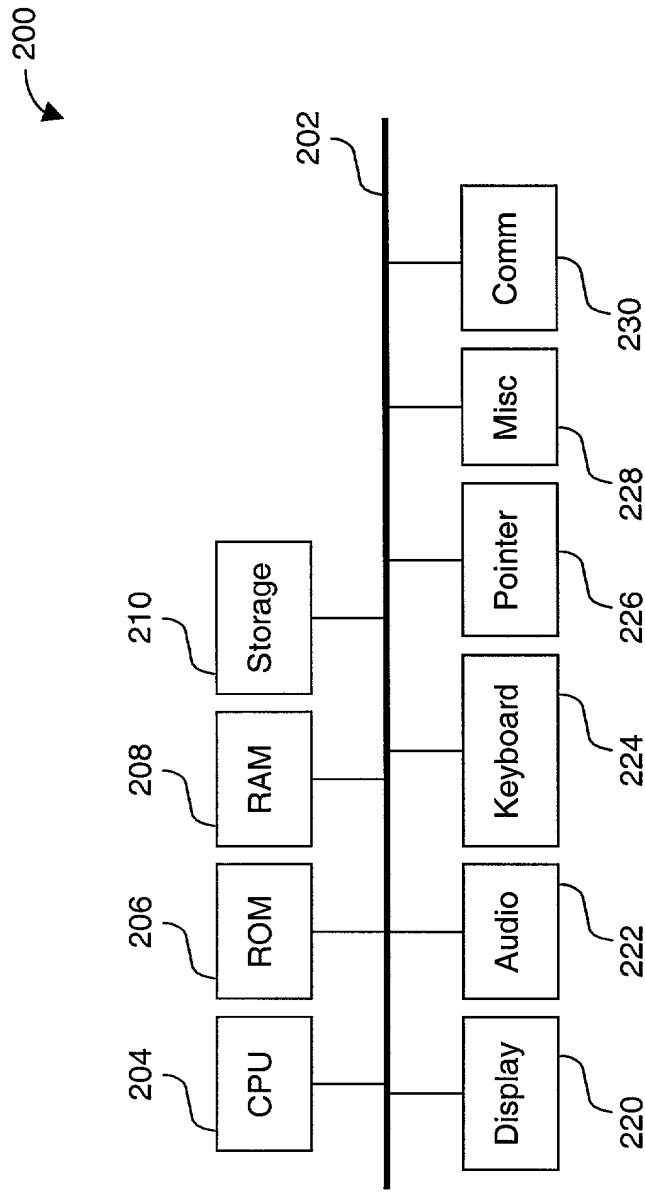


FIG. 2

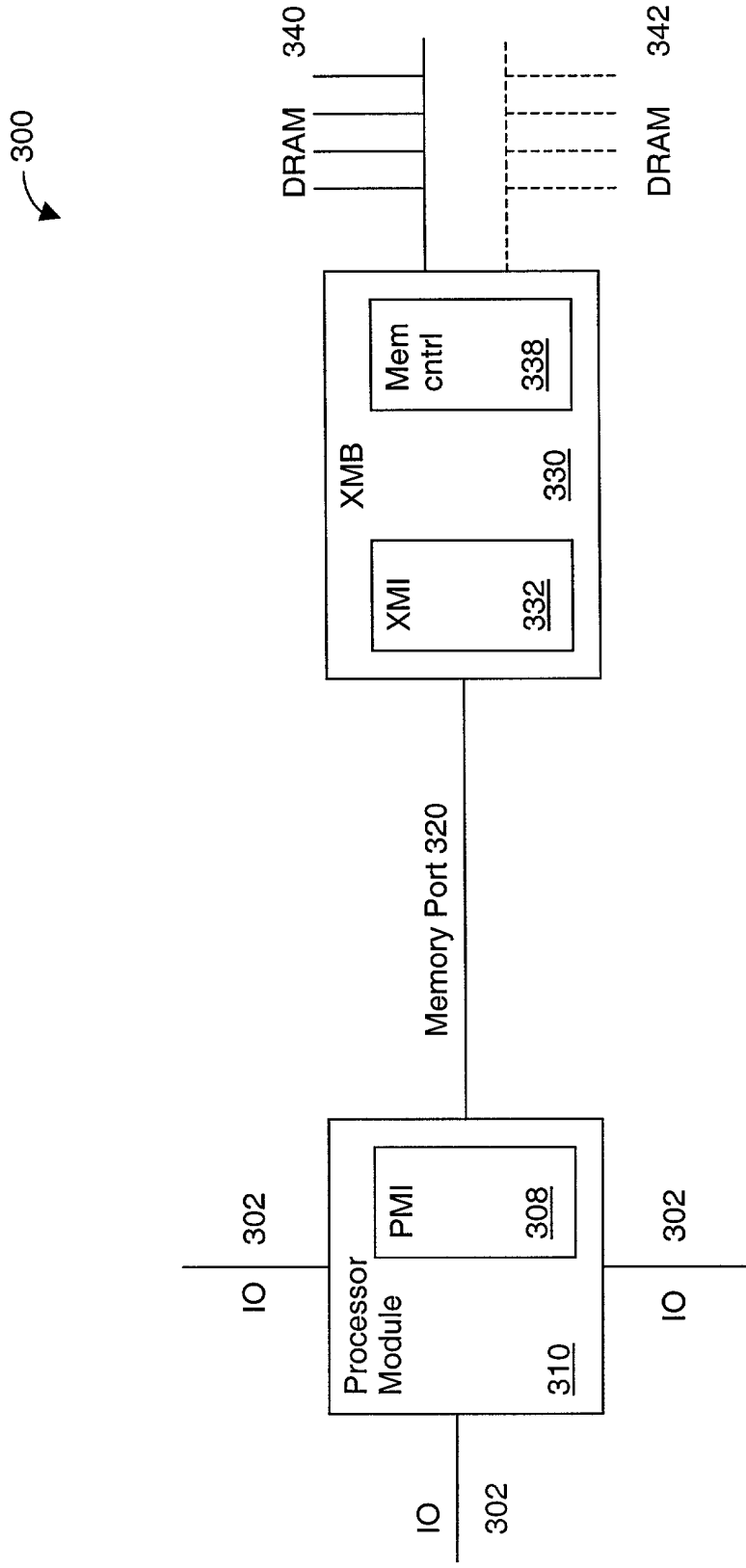


FIG. 3

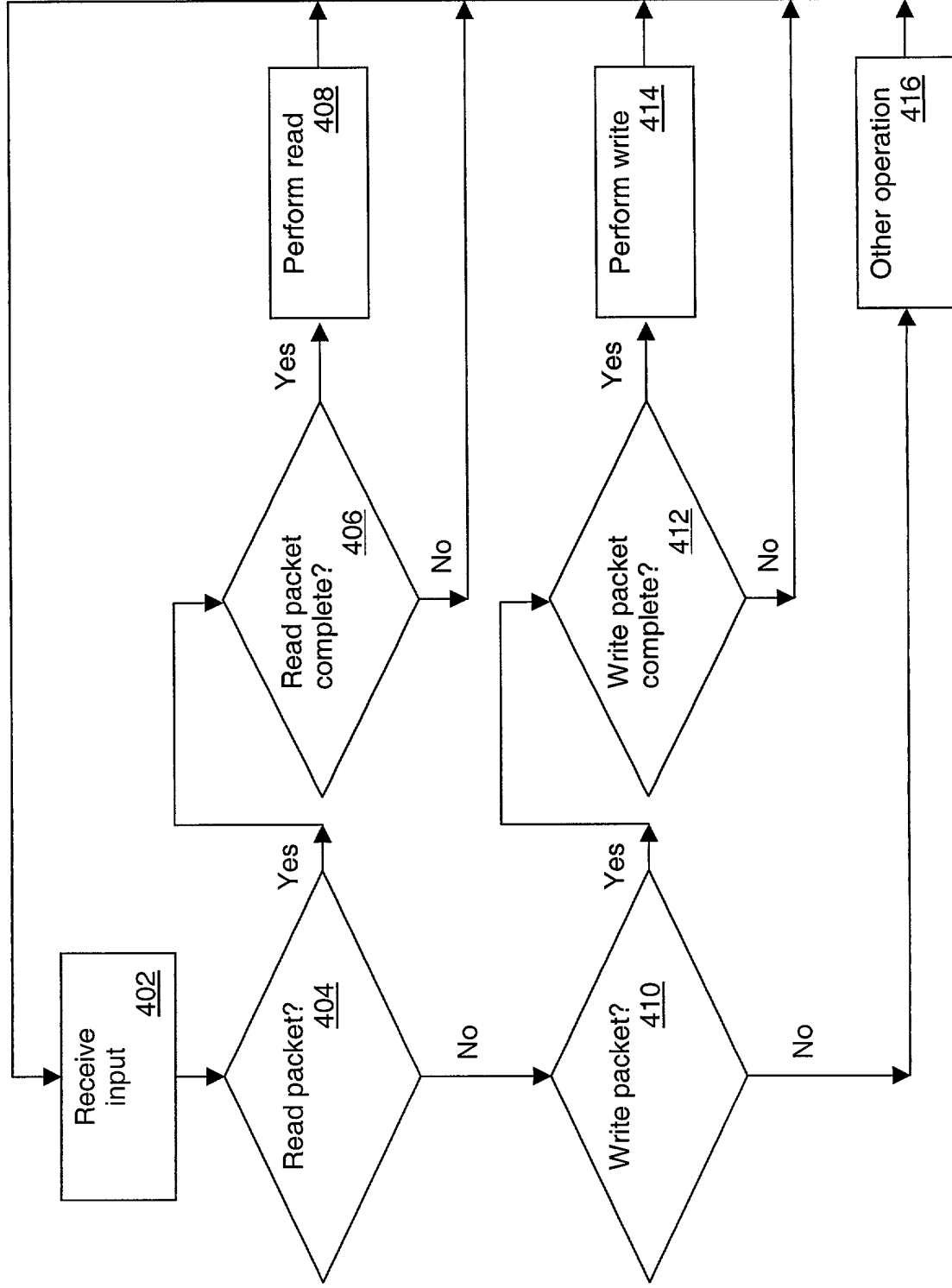


FIG. 4A

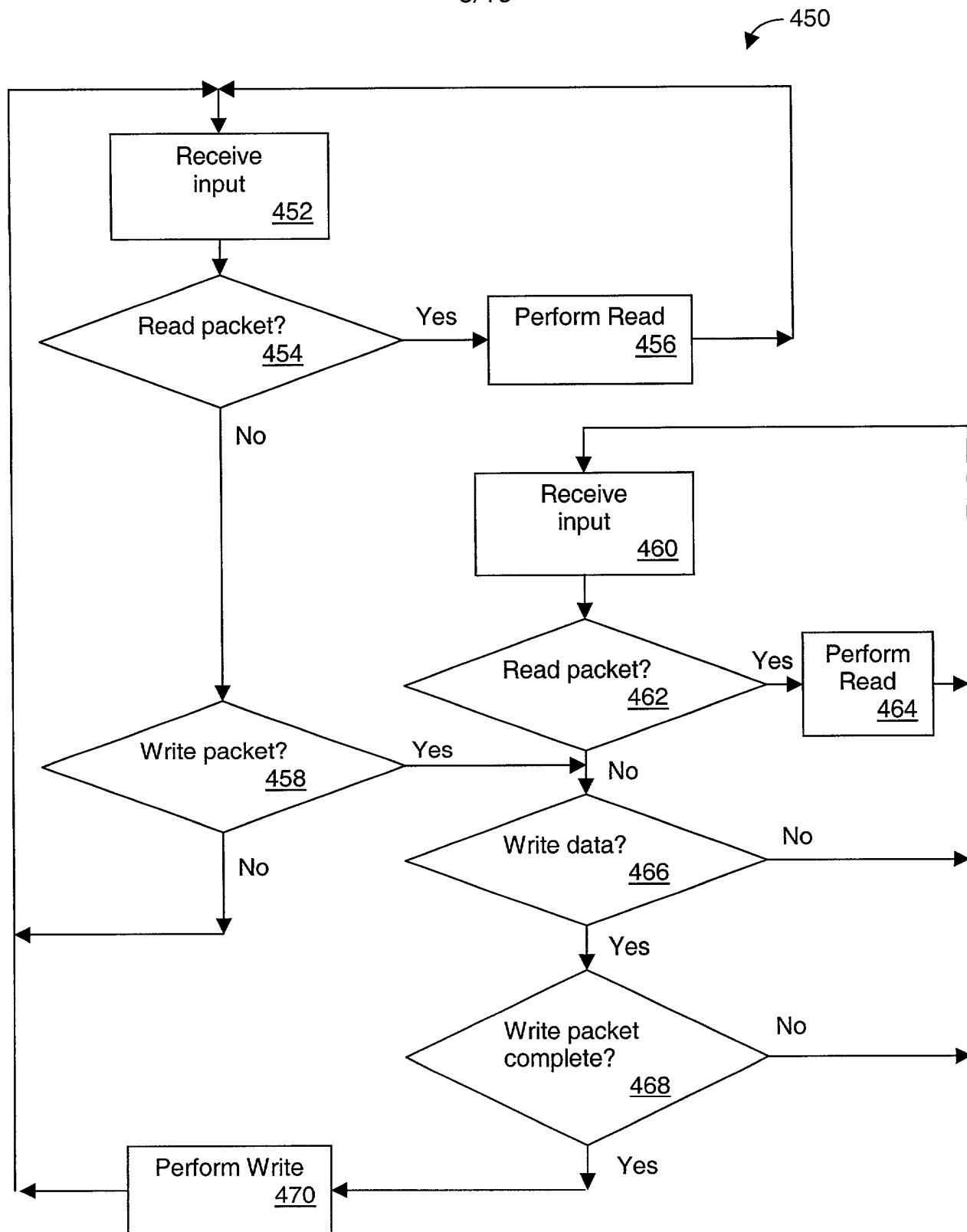


FIG. 4B

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500

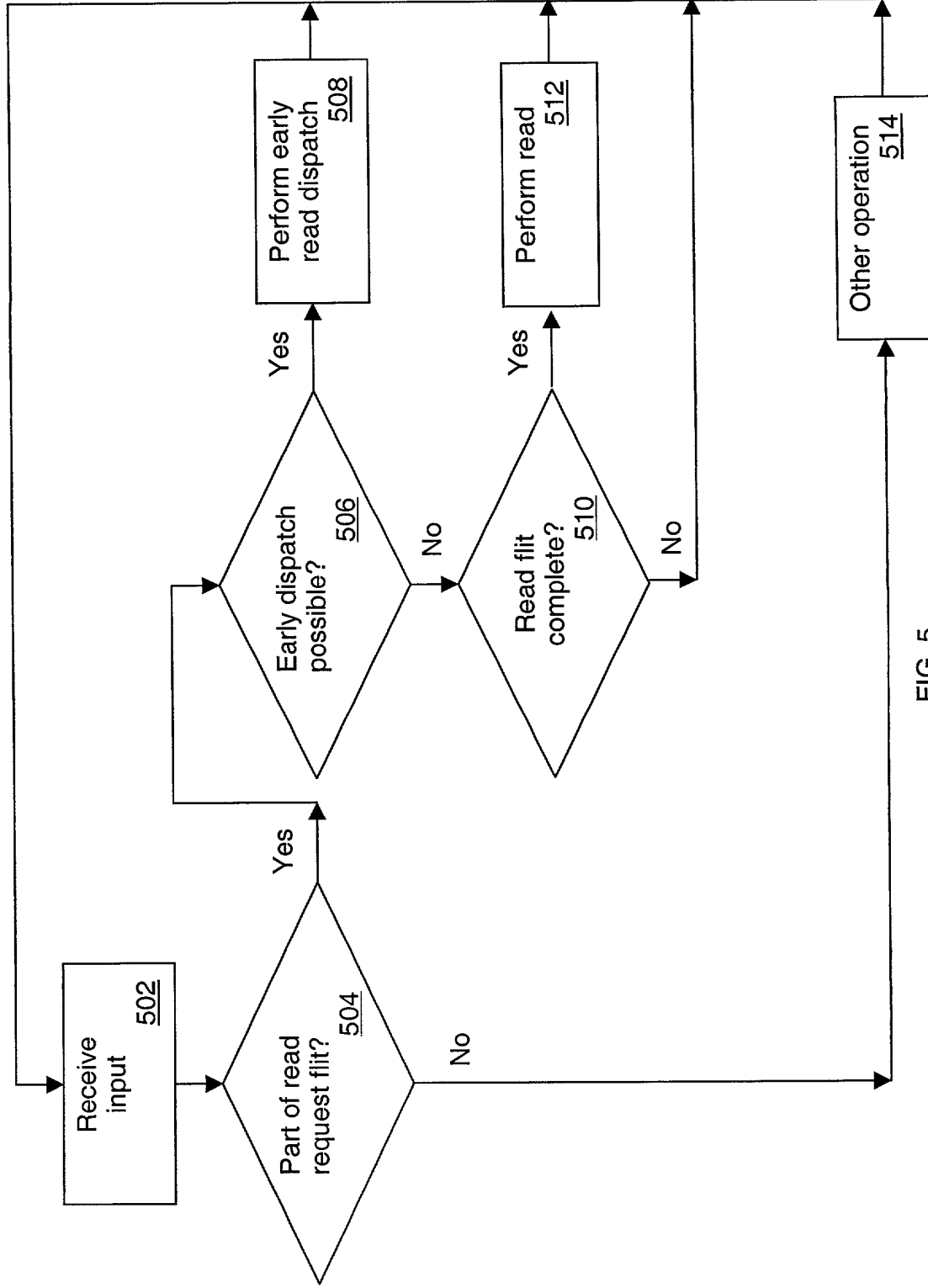


FIG. 5

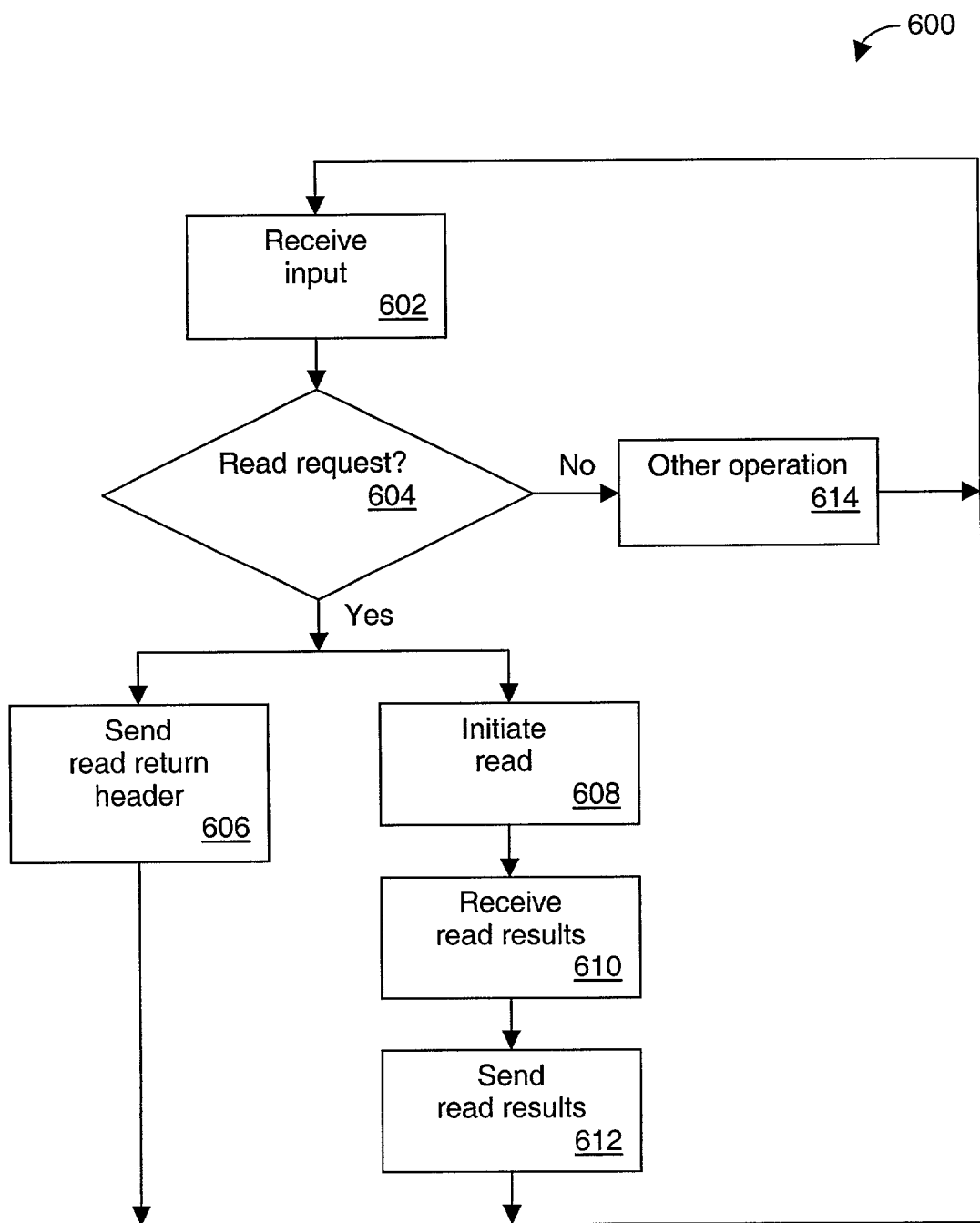


FIG. 6A

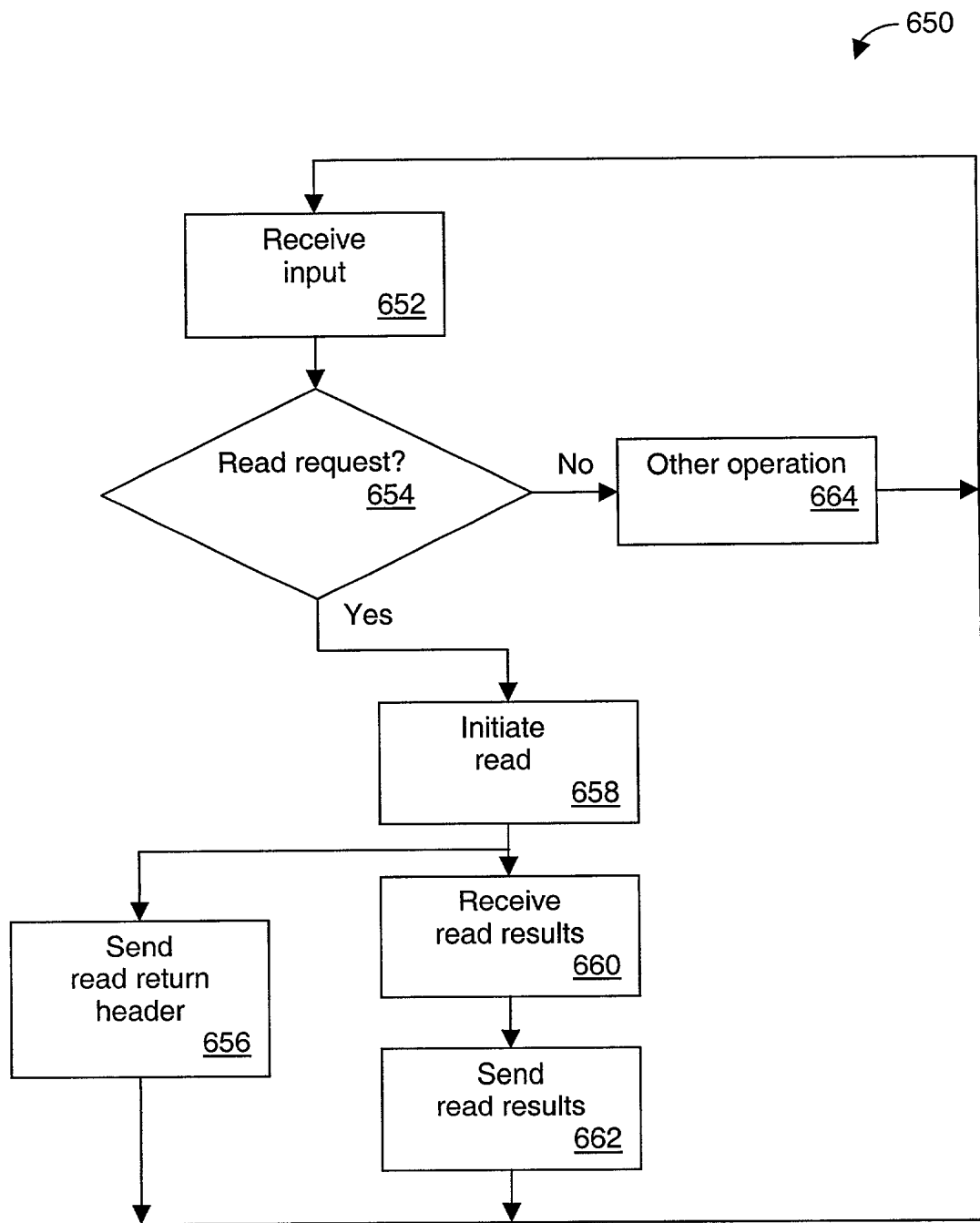


FIG. 6B



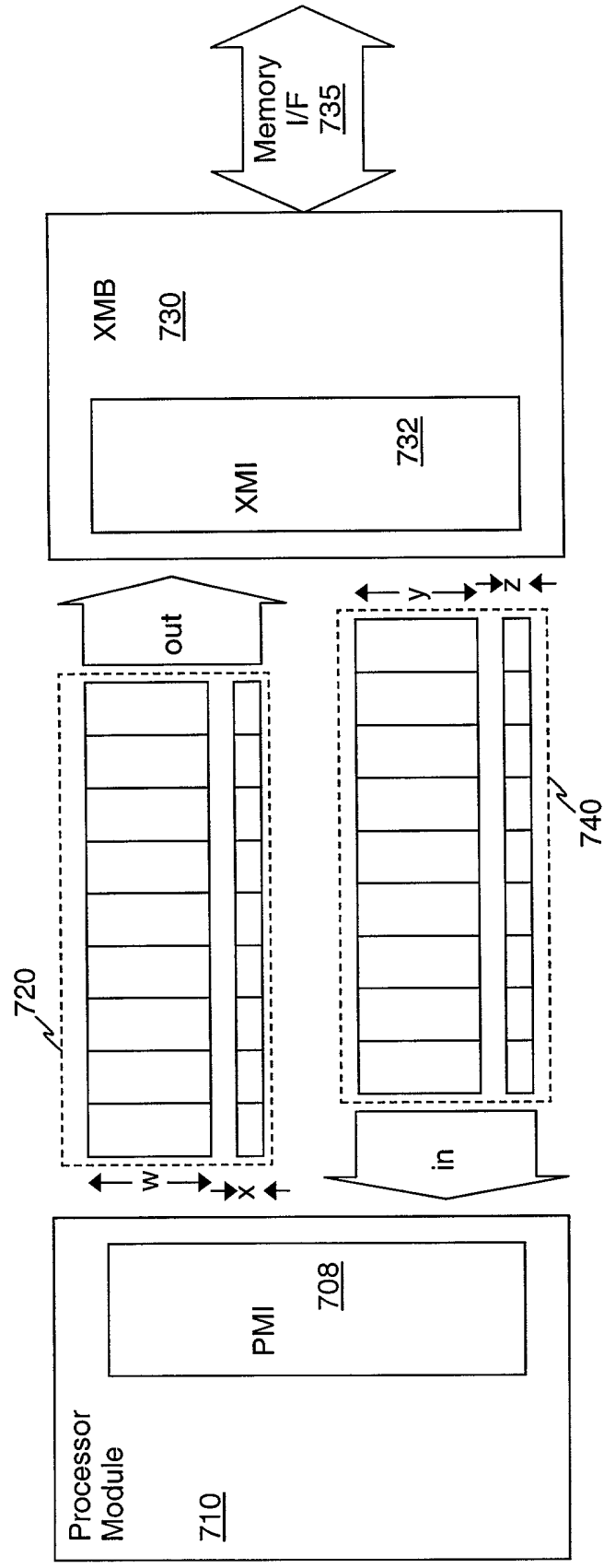


FIG. 7

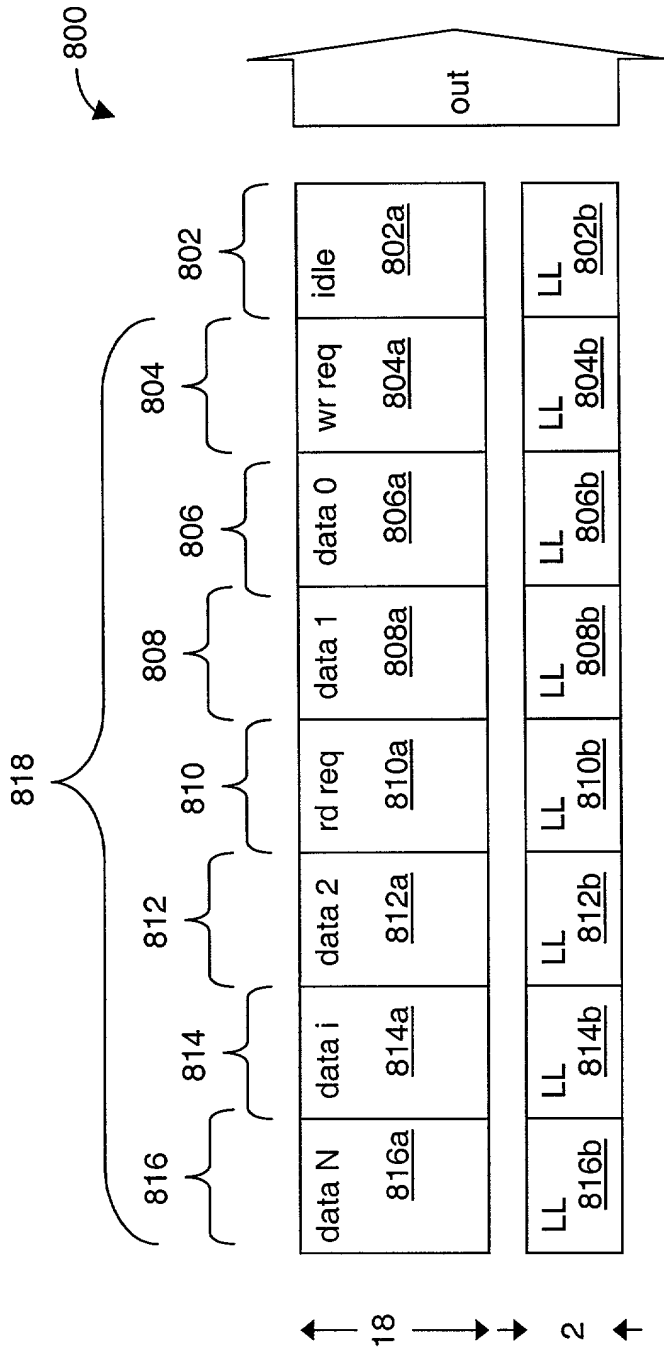


FIG. 8

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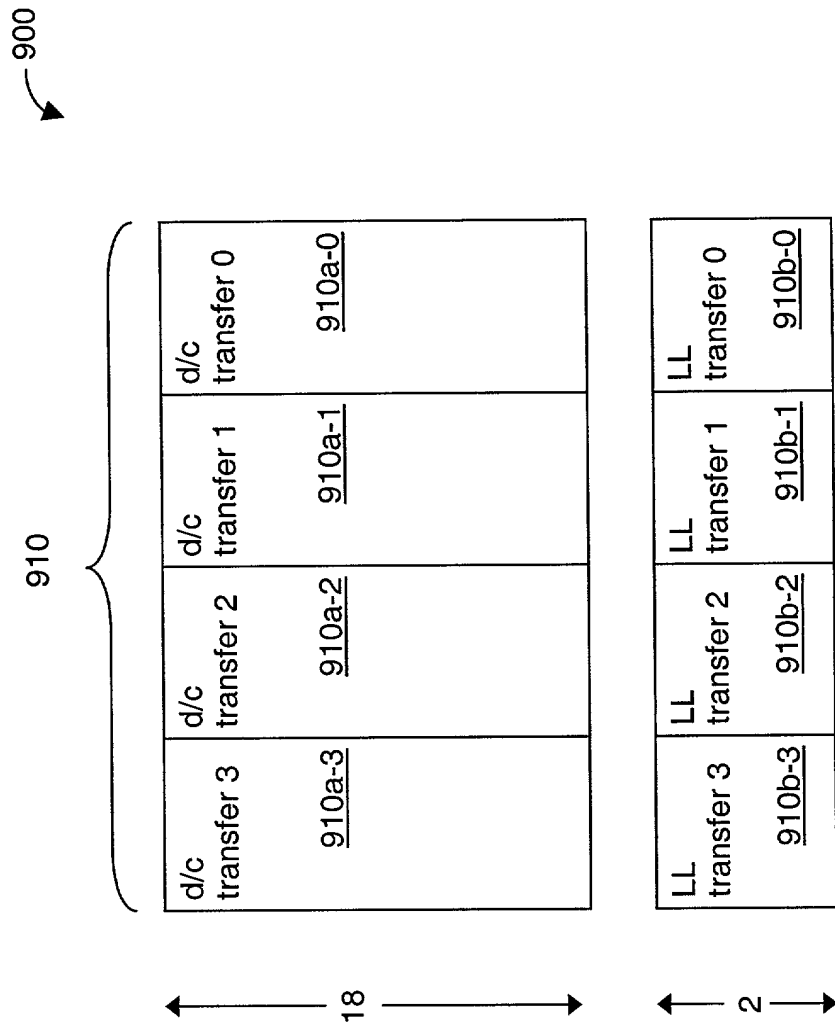


FIG. 9

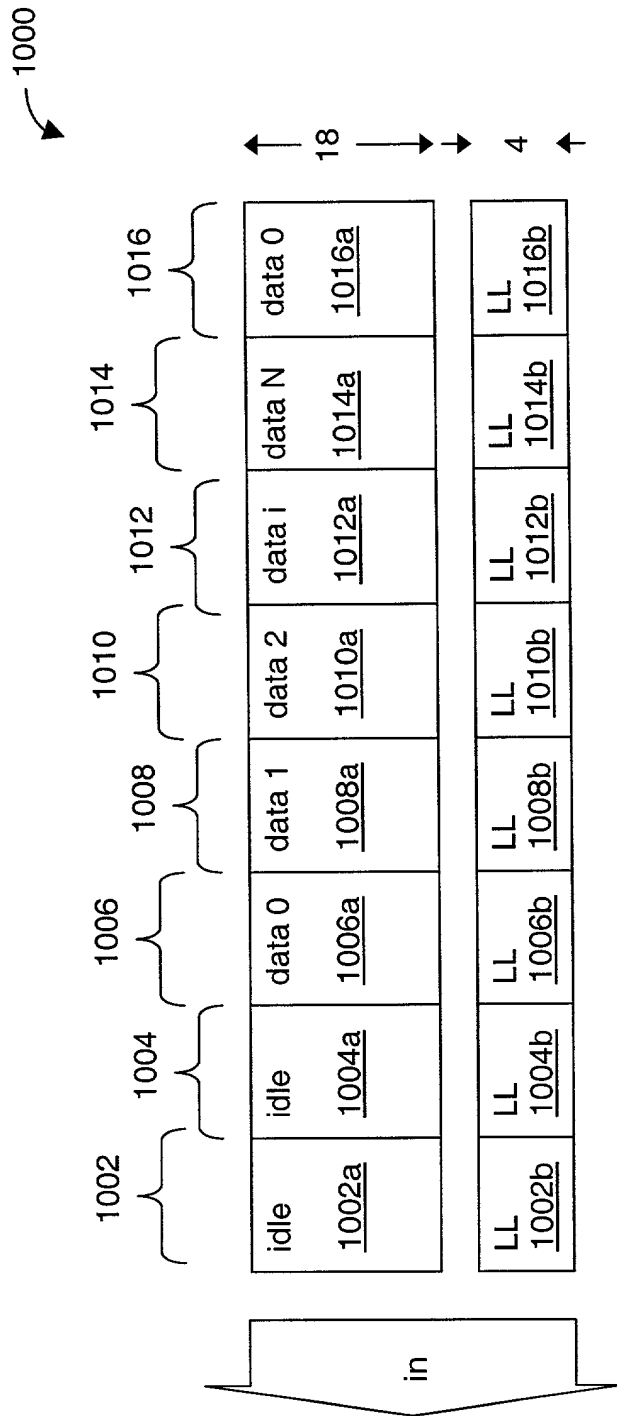


FIG. 10

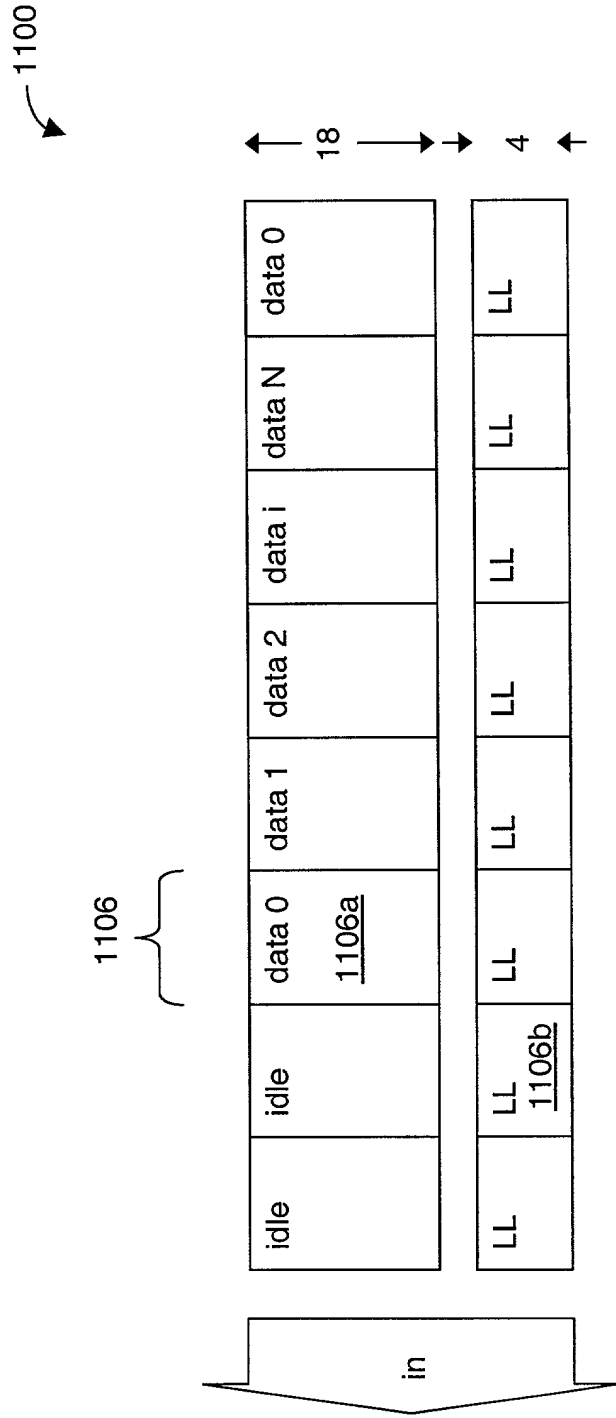


FIG. 11

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1200

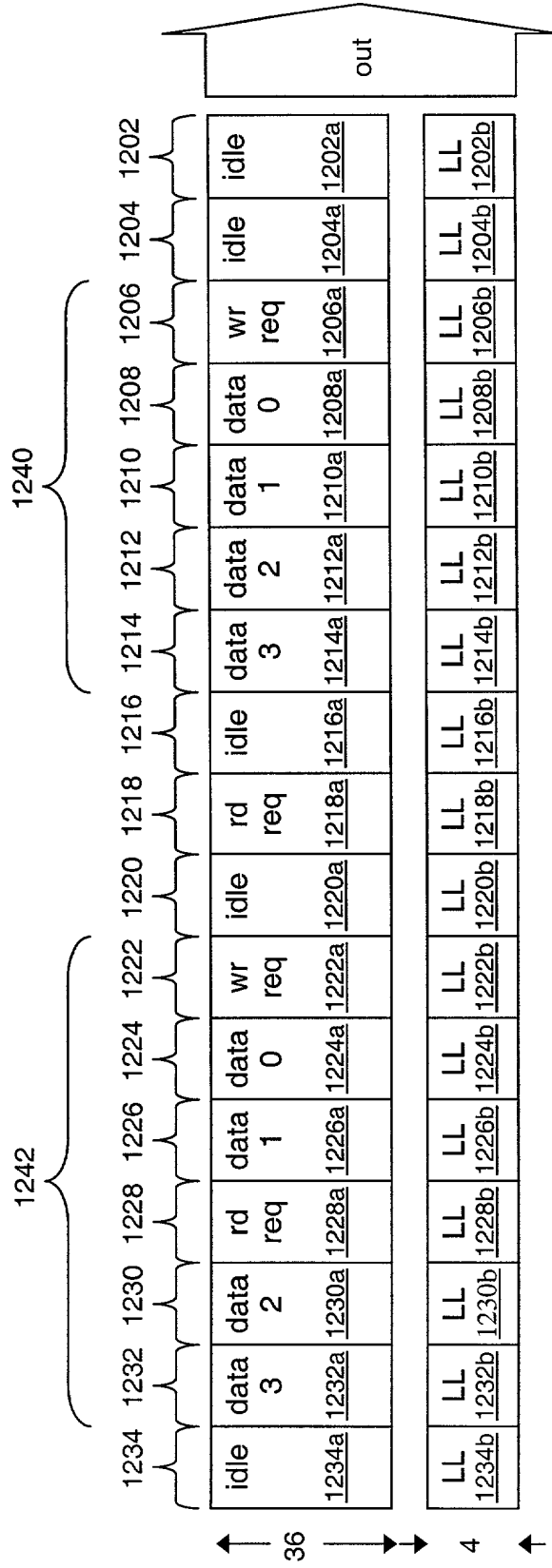


FIG. 12

↓Transfer	BITS 17:0
0	Lower Order Address Bits and Read/Write Command
1	Higher Order Address Bits and Early Read Indicator
2	Command Destination, Offset from Address, Transaction ID, Check Bits, Mask Bits, Stream ID,
3	Size Bits, Cancel Command, Priority, etc.

FIG. 13

↓Transfer	BITS 17:0
0	Lower Order Address Bits and Read/Write Command
1	Higher Order Address Bits and Early Read Indicator
2	Command Destination, Offset from Address, Transaction ID, Check Bits, Mask Bits, Size Bits, etc.
3	

FIG. 14



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1500

↓Transfer	BITS 17:0
0	Lower Order Configuration Address Bits and Read/Write Command
1	Higher Order Configuration Address Bits and Early Read Indicator
2	Command Destination, Offset from Address, Transaction ID, Check Bits, Mask Bits, etc.
3	

FIG. 15

1600

LL signals	Transfers 0:3
0	Info and Check Bits
1	Header, Tail, and Check Bits
2	Extended Mode Bits
3	

FIG. 16

1700

LL signals	Transfers 0:3
0	Type and Check Bits
1	
2	Info and Check Bits
3	

FIG. 17

1800

LL signals	Transfers 0:3
0	Tag, Control, and Check Bits
1	
2	Tag, Info, and Check Bits
3	

FIG. 18

1900

FIG. 19

2000

LL signal

FIG. 20